

# Power Quality Improvement Using a New Structure of Fault Current Limiter

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**Abstract**-In this paper, power quality improvement by using a new structure of non superconducting fault current limiter (NSFCL) is discussed. This structure prevents voltage sags on Point of Common Coupling (PCC) just after fault occurrence, because of its fast operation. On the other hand, previously used structures produce harmonics on load voltage and have ac losses in normal operation. New structure has solved this problem by using dc voltage source. The proposed structure is simulated using PSCAD/EMTDC software and simulation results are presented to validate the effectiveness of this structure.

## I. INTRODUCTION

Electric power quality can be defined as the capacity of an electric power system to supply energy for a load in acceptable quality. Consequently, power quality problems have become a major concern in the power systems [1, 2].

Voltage sag is a rather old power quality problem that nowadays becomes important because of sensitive loads growth [3]. Worldwide experience demonstrates that short circuit faults are the main origin of voltage sags. This problem appears especially on buses that are connected to radial feeders. Since the voltage sag during the fault is proportional to the short circuit current, an effective fault current limitation by means of a device connected at the beginning of the most exposed radial feeders will limit the expected voltage sag and improve the system power quality [4].

Superconducting FCL structures offer good ways to control the fault current levels due to their variable impedance at normal and fault conditions. Unfortunately, because of high technology and cost of superconductors, these devices are not commercially available. Therefore, replacing the superconducting coil with non superconducting coil in FCL makes it simpler and much cheaper. It should be noted that, the main drawback of NSFCL is power losses which is negligible in comparison with the total power, provided by distribution feeder [5].

In this paper, primarily main power quality problem, i.e. voltage sag, is discussed. Then in the section III proposed NSFCL circuit is introduced and its operation in the simplified power system is explained briefly. Then, the PSCAD/EMTDC software is applied to investigate the operational behavior of the NSFCL in this power system and simulation results are analyzed. Finally, it will be shown that our proposed structure is useful for power quality improvement because of voltage sag mitigating and low harmonic distortion in distribution systems.

## II. VOLTAGE SAG STUDY IN RADIAL POWER SYSTEM

Fig. 1 shows a simplified radial power system. Feeder F1 supplies a sensitive load. With a fault in feeder F2, Point of Common Coupling (PCC) voltage reduces sharply. In case of three phase fault at the beginning of line, PCC voltage becomes almost zero and sensitive load supplying interrupts.

Positive sequence equivalent circuit of such system is shown in Fig. 2. To calculate the voltage sag, simple voltage divider method is introduced in [6].

PCC voltage can be expressed by (1):

$$V_{PCC} = \frac{Z_K}{Z_K + (Z_S + Z_t)} V_S \quad (1)$$

Where:

$Z_t$  : Transformer impedance

$Z_S$  : Source impedance

$V_S$  : Source voltage

$Z_K$  : Equivalent impedance of parallel feeders i.e.:

$$Z_K = (Z_{L1} + Z_{SL}) \parallel (Z_{L2} + Z) \quad (2)$$

In normal state,  $Z_K$  is greater than  $(Z_S + Z_t)$ . So, PCC voltage almost is equal to source voltage. At fault condition in feeder F2,  $Z_K$  changes as follow:

$$Z_K = (Z_{L1} + Z_{SL}) \parallel (Z_{L2} + Z_F) \quad (3)$$

Where:

$Z_F$  : Fault impedance

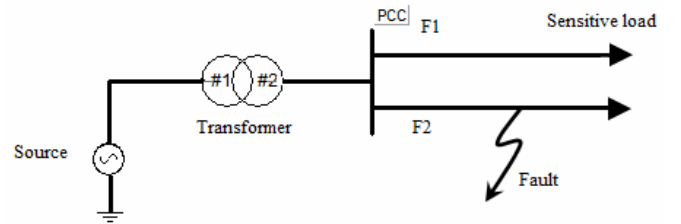


Figure 1. A simplified radial power system

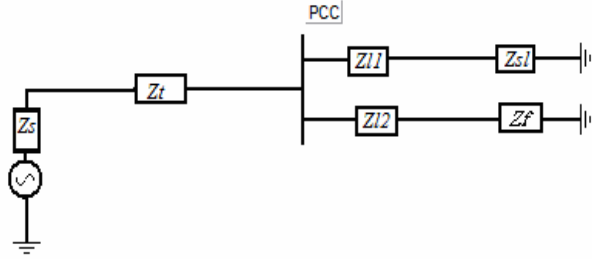


Figure 2. Positive sequence equivalent circuit of study system at fault condition

In three phase fault condition,  $Z_F$  equals to zero and according to (3),  $Z_K$  will be small.

Consequently, referring to (1), magnitude of PCC voltage at fault interval falls strongly and sensitive load experiences a voltage interruption. To prevent this voltage sag, a proper solution, is introducing large limiting impedance between PCC and the fault. This solution is base of FCL's operation.

### III. PROPOSED NSFCL CONFIGURATION AND ITS OPERATION

Fig. 3 shows the circuit topology of proposed FCL which is composed of following part: Diode rectifier bridge, dc limiting reactor ( $L_{dc}$ ) (Note that, its natural resistance ( $R_{dc}$ ) is involved too.), IGBT switch, free wheeling diode ( $D_5$ ), dc voltage source and finally shunt impedance ( $R_{sh} + j\omega L_{sh}$ ).

In normal condition, IGBT is on.  $L_{dc}$  is charged to peak of line current and therefore behaves as short circuit. Because of using semiconductor devices (diodes and IGBT) and non superconducting reactor, there are some voltage drops on bridge. Dc voltage source is utilized to compensate voltage drops on diode, IGBT and  $R_{dc}$ . So, its magnitude can be achieved by (4) as follow:

$$V_{dc} = R_{dc}I_{dc} + 2V_{DF} + V_{IGBT} \quad (4)$$

It is important to note that dc voltage source can be provided by rectifiers.

Therefore, total voltage across FCL becomes almost zero and as result, FCL doesn't affect normal operation of system.

As fault occurs, line current begins to increase, but  $L_{dc}$  limits its increasing speed. When the current reaches to the maximum permissible fault current ( $I_m$ ), control system of IGBT turns it off. So, the bridge retreats from feeder and shunt impedance enters to faulted line and limits fault current. At this time free wheeling diode discharges  $L_{dc}$ . In fact, free wheeling diode is used to provide free route for dc reactor current.

After fault removal, IGBT turns on again and system returns to normal state.

Previously introduced structures for this application have used two numbers of thyristors at bridge branches instead of IGBT inside bridge (dc current route). Therefore, they have more complicated control system. In addition, they have no idea about voltage distortion caused by FCL. But, in this

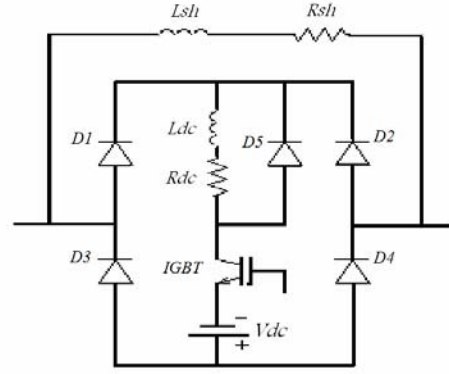


Figure 3. Proposed NSFCL topology

structure, dc voltage source placed inside bridge resolves this problem that is explained completely at section V.

From other view point, without compensating the voltage drop across rectifier bridge, a current flows from shunt branch. Consequently, there are ac losses in the resistance of shunt impedance.

By making voltage drop on FCL almost zero, ac loss in proposed FCL is very lower than previous structures. In this case it is possible to place a large resistor ( $R_{sh}$ ) in series with  $L_{sh}$  as shown in Fig. 3. This leads to good limitation of current and reduction of its transient at fault condition.

Next sections indicate the effectiveness of these solutions to reduce voltage sag, harmonic injection and ac power losses, consequently improve power quality.

### IV. EFFECT OF PROPOSED NSFCL ON VOLTAGE SAG AND SIMULATION RESULT

As fault occurs at F2, Fig. 1, without using FCL, PCC voltage drops terribly. When FCL is installed at F2, not only reduces fault current, but also restore the non faulted feeder voltage to a normal level. In fact, during a short circuit, the voltage drop causes a corresponding drop in F1; the FCL can help to improve the power quality and the reliability of the supply network. In this section, analytical analysis of proposed NSFCL with simulation results is expressed.

Power equipment data are as follows:

Source: 20 kV, 10 MVA, 50Hz, 1.608  $\Omega$

Transformer: 20 kV/6.6 kV, 10 MVA, 0.1 pu

Distribution feeder data:

Impedance of F1 = 0.314  $\Omega$

Impedance of F2 = 0.157  $\Omega$

DC reactor of NSFCL,  $L_{dc}$  = 0.01 H

DC resistance of NSFCL,  $R_{dc}$  = 0.03  $\Omega$

Shunt reactor of NSFCL,  $L_{sh}$  = 0.08 H

Shunt resistance of NSFCL,  $R_{sh}$  = 5  $\Omega$

Load data in feeder F2:

Resistance = 15  $\Omega$

Inductance = 0.1 H

Parameters of NSFCL are chosen in a way that fault current be close to feeder's nominal current.

As shown in Fig. 4, in a fault condition, PCC voltage and power transferring to sensitive load drops without FCL. With placing proposed FCL in outset of F2, as fault happens, FCL inserts large impedance into faulted line and prevents voltage sag at PCC.

Fig. 5 shows PCC voltage and sensitive load power in this state. In the first moments of fault, slight distortion appears on PCC voltage waveform caused by IGBT operation and inserting shunt impedance into line. After that PCC voltage sag will be less than 1%. The power of sensitive load in this interval hasn't any sensible change.

In comparison with operation of structures introduced in [3], [7] and [8], using IGBT switch at dc current route instead of thyristor at bridge branches, in proposed NSFCL, leads to mitigation of sag and distortion in PCC voltage just after fault occurrence (Fig. 6).

As shown in simulation results, proposed NSFCL can resolve voltage sag problem properly.

Fig. 7 shows line current of F2, dc reactor and shunt impedance current ( $i_L(\omega t)$ ,  $i_{dc}(\omega t)$  and  $i_{sh}(\omega t)$  respectively). As shown in Fig. 7(b), between fault occurrence instant ( $t_0$ ) and line current rising to its normal condition's peak instant ( $t_1$ ), dc reactor current doesn't change. From instant  $t_1$  to  $t_2$  (IGBT operation instant), dc reactor charges according to differential equation (5):

$$\begin{cases} \omega L_{dc} \frac{di_{dc}(\omega t)}{d\omega t} + R_{dc} i_{dc}(\omega t) + 2V_{DF} + V_{IGBT} = V_{PCC} + V_{dc} \\ i_{dc}(\omega t = \omega t_1) = I_{dc} \end{cases} \quad (5)$$

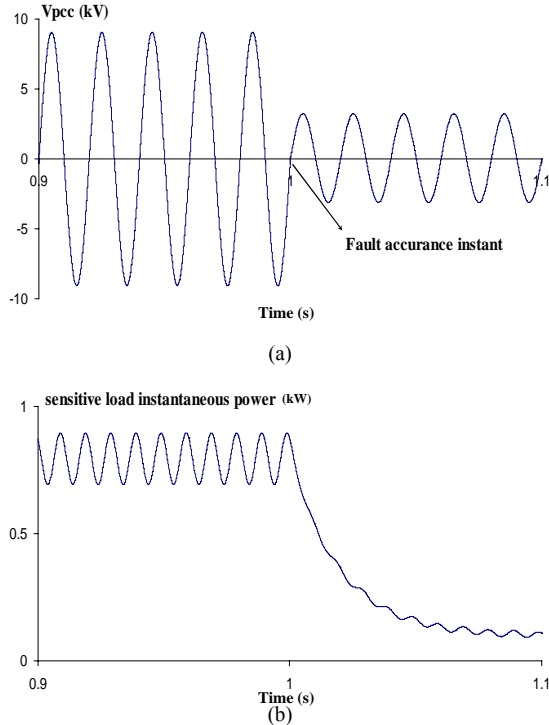


Figure 4. (a) PCC voltage and (b) sensitive load instantaneous power without NSFCL

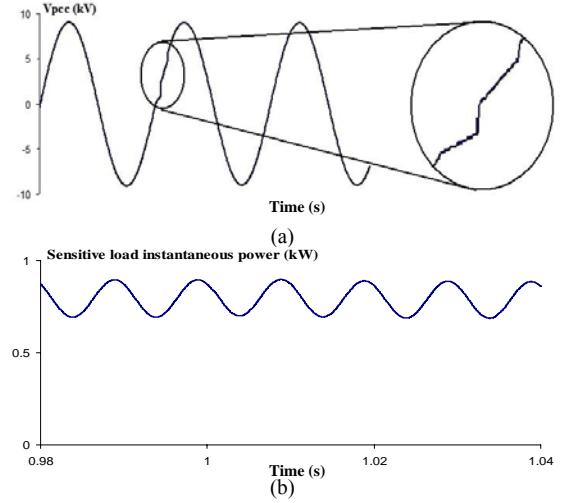


Figure 5. (a) PCC voltage and (b) sensitive load instantaneous power with proposed NSFCL

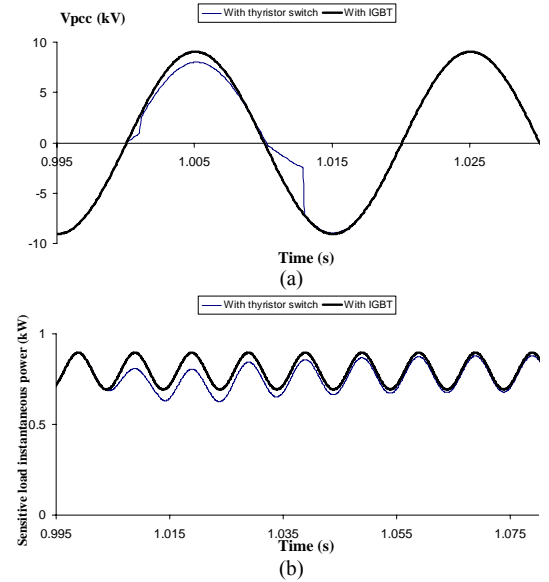


Figure 6. (a) PCC voltage and (b) sensitive load instantaneous power waveforms before and after optimization

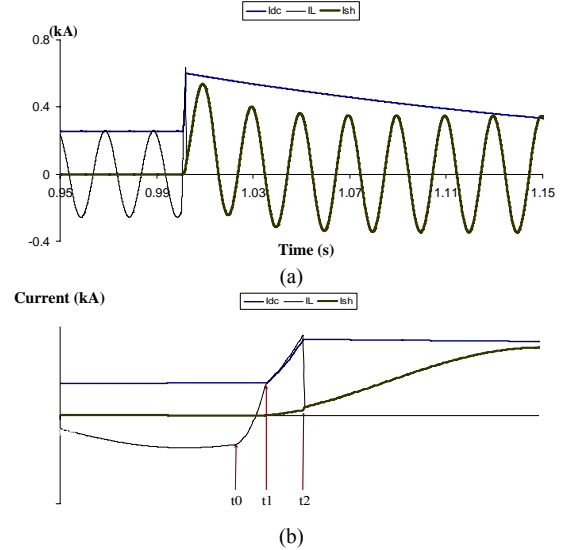


Figure 7. (a) line, dc reactor and shunt impedance current and (b) with detailed

Where:

$I_{dc}$ : dc reactor current at normal condition that equals to the peak of line current.

$i_{dc}(\omega t)$ : dc reactor current between  $t_1$  to  $t_2$ .

$V_{DF}$ : Forward voltage drop on diodes.

$V_{IGBT}$ : Forward voltage drop on IGBT.

$V_{PCC} = V_P \sin(\omega t)$

$V_{dc}$ : dc voltage source magnitude, see (4).

With solving (5):

$$i_{dc}(\omega t) = A e^{\frac{-R_{dc}}{\omega L_{dc}} \omega(t-t_1)} + B \sin(\omega t - \varphi_{dc}) + K \quad (6)$$

Where:

$$\begin{cases} A = I_{dc} - \frac{V_P}{\sqrt{R_{dc}^2 + \omega^2 L_{dc}^2}} \sin(\omega t_1 - \varphi_{dc}) + \frac{2V_{DF} + V_{IGBT} - V_{dc}}{R_{dc}} \\ B = \frac{V_P}{\sqrt{R_{dc}^2 + \omega^2 L_{dc}^2}} \\ K = \frac{V_{dc} - 2V_{DF} - V_{IGBT}}{R_{dc}} \\ \varphi_{dc} = \arctan\left(\frac{\omega L_{dc}}{R_{dc}}\right) \end{cases} \quad (7)$$

In addition, at this interval, voltage across FCL increase shunt impedance current. Differential equation of this current is expressed by (8):

$$\omega L_{sh} \frac{di_{sh}(\omega t)}{d\omega t} + R_{sh} i_{sh}(\omega t) = V_{PCC} \quad (8)$$

Initial value of  $i_{sh}(\omega t)$  is zero. Then:

$$i_{sh}(\omega t) = A e^{\frac{-R_{sh}}{\omega L_{sh}} \omega(t-t_1)} + B \sin(\omega t - \varphi_{sh}) \quad (9)$$

Where:

$$\begin{cases} A = -\frac{V_P}{\sqrt{R_{sh}^2 + \omega^2 L_{sh}^2}} \sin(\omega t_1 - \varphi_{sh}) \\ B = \frac{V_P}{\sqrt{R_{sh}^2 + \omega^2 L_{sh}^2}} \\ \varphi_{sh} = \arctan\left(\frac{\omega L_{sh}}{R_{sh}}\right) \end{cases} \quad (10)$$

IGBT control strategy is based on maximum permissible fault current ( $I_m$ ). Between  $t_1$  to  $t_2$ , line current ( $i_L(\omega t)$ ) equals to  $i_{dc}(\omega t)$  plus  $i_{sh}(\omega t)$  (Fig.7(b)). When IGBT current exceeds from  $I_m$ , control system of IGBT turns it off. If in (6),  $i_{dc}(\omega t)$  be equal to  $I_m$ , IGBT operation instant ( $t_2$ ) will be calculated. After  $t_2$ , diode bridge retreats and shunt

impedance limits fault current. Until fault clearance instant and turning on of IGBT, line current follows (9). In addition, at this interval,  $i_{dc}(\omega t)$  is discharged by  $D_5$  as following equation:

$$\begin{cases} \omega L_{dc} \frac{di_{dc}(\omega t)}{d\omega t} + R_{dc} i_{dc}(\omega t) = 0 \\ i_{dc}(\omega t = \omega t_2) = I_m \end{cases} \quad (11)$$

As a result:

$$i_{dc}(\omega t) = I_m e^{\frac{-R_{dc}}{\omega L_{dc}} \omega(t-t_2)} \quad (12)$$

It is important to note that (9) is composed of two parts; exponential and sinusoidal. Exponential part causes a transient in line current (as shown in Fig. 7(a)) that duration of this transient depends on shunt impedance time constant ( $L_{sh}/R_{sh}$ ). In case that shunt branch is consist of reactance only (e.g. in [7]), time constant becomes greater and as result transient of current last more time. By placing a large resistance in series with the reactance, current transient damps in short time.

## V. HARMONIC STUDY

As explained previously, using the dc voltage source in proposed structure and compensation of voltage drop on the power electronic devices and dc reactor resistance reduces THD of voltage waveform.

Fig. 8 shows load voltage at normal operation of power system with and without dc voltage source and Fig. 9 shows the frequency spectrum of load voltage.

By using proposed NSFCL the distortions of voltage waveform decreases to lower values, as shown in Fig. 8 and Fig. 9. Simulation results prove this statement as follows: THD of load voltage in case of NSFCL without dc voltage source: 2.789%

THD of load voltage in case of NSFCL with dc voltage source: 0.117%

It is important to note that the THD of load voltage is near to zero for proposed structure.

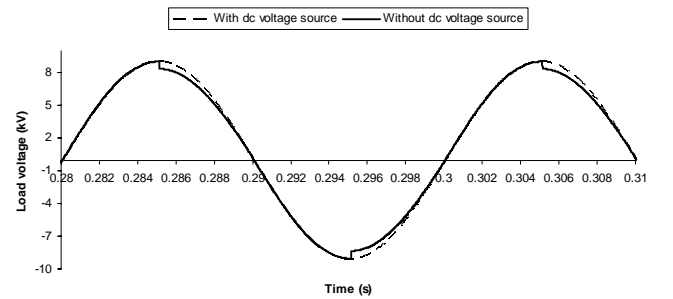


Figure 8. load voltage at normal operation of power system with and without dc voltage source

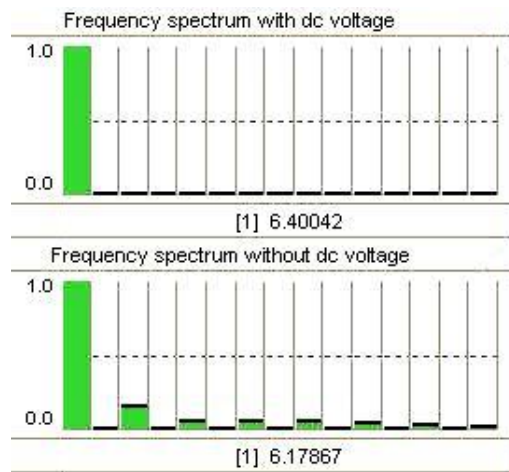


Figure 9. Frequency spectrum of load voltage

## VI. CONCLUSION

Today the problem of power quality improvement is very important. In this paper the new topology of a NSFCL structure is introduced. Power quality improvement and fault current limiting operation due to the control method were analyzed through the computer simulation. Proposed NSFCL is capable of mitigating voltage sags to acceptable levels and has high speed because of using IGBT switch instead of thyristors. Note that the control system of this structure is more

simpler than previous ones, because it uses IGBT at dc current path instead of two numbers of thyristor at the bridge branches. In addition, dc voltage source placed in FCL structure reduces its THD and ac losses in normal operation. In general this type of NSFCL is useful for power quality improvement because of voltage sag mitigating and low harmonic distortion in distribution systems.

## REFERENCES

- [1] Timothy J. Browne, Gerald T. Heydt. "Power Quality as an Educational Opportunity," *IEEE Trans. Power Del.*, vol. 23, no. 2, pp. 814-815, May 2008.
- [2] Nesimi Ertugrul, Ameen M. Gargoom, Wen. L. Soong. "Automatic Classification and Characterization of Power Quality Events," *IEEE Trans. Power Del.*, vol. 23, no. 4, pp. 2417-2425, October 2008.
- [3] M. Abapour, Seyed Hossein Hosseini, M. Tarafdar Hagh. "Power Quality Improvement by Use of a New Topology of Fault Current Limiter," *ECTI-CON.*, pp.305-308, 2007.
- [4] Stefano Quaia, Fabio Tosato. "Reducing Voltage Sags Through Fault Current Limitation," *IEEE Trans. Power Del.*, vol. 16, no. 1, pp.12-17, January 2001.
- [5] Mehdi Abapour, Mehrdad Tarafdar Hagh. "Nonsuperconducting Fault Current Limiter With Controlling the Magnitudes of Fault Currents," *IEEE Trans. Power Electronics.*, vol. 24, no. 3, pp. 613-619, March 2009.
- [6] L.E. Conrad. "Proposed Chapter 9 for predicting voltage sags (Dips) in revision to IEEE Std. 493, the gold book," *IEEE Transactions on Industry Applications*, pp. 805-821, May/June 1994.
- [7] D. Jiang, Z. Lu, Z. Wu. "Anewtopology of fault-current limiter and its parameters optimization," *Proc. IEEE Power Electron. Specialists Conf.*, pp. 462-465, June 2003.
- [8] J. Daozhuo, C. Gang, C. Yonghua, "Study on a novel solid state fault current limiter with bypass reactor," *Proc. Chinese Soc. Electrical Eng*